IN THE CLAIMS

1. (Previously Presented) A method of fabricating an interconnect structure, comprising:

(a) providing a substrate having a film stack comprising sequentially formed on the substrate a first barrier layer, a conductive layer embedded in a first dielectric layer, a second barrier layer, a second dielectric layer, and a cap layer;

(b) etching a via hole in the cap layer and the second dielectric layer;

(c) filling a portion of a depth of the via hole with a masking material;

(d) etching in-situ the cap layer, a trench in the second dielectric layer, the masking material, and the second barrier layer, by providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts while etching during at least a portion of step (d); and

(e) metallizing the via hole and the trench.

2. (Original) The method of claim 1 wherein the cap layer comprises SiO_xN_y, where x and y are integers.

3. (Previously Presented) The method of claim 1 wherein the first dielectric layer and the second dielectric layer comprise at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass.

4. (Previously Presented) The method of claim 1 wherein the first barrier layer and the second barrier layer comprise at least one of SiO_2, SiC, and Si_3N_4.

5. (Original) The method of claim 1 wherein the conductive layer comprises at least one of Cu, Al, Ta, W, Ti, TaN, and TiN.

6. (Original) The method of claim 1 wherein the masking material is selected from a group consisting of an organic material and photoresist.

7. (Original) The method of claim 1 wherein the step (b) further comprises:

forming a first patterned etch mask on the cap layer to define the via hole;

etching the via hole providing CF_4 and N_2 at a flow ratio $CF_4:N_2$ in a range from 1:1 to 1:5; and

stripping the first patterned etch mask.

8. (Original) The method of claim 1 wherein the step (c) further comprises:

applying the masking material to the substrate to fill the via hole; and

etching back the masking material until the masking material is removed from the via hole to a pre-determined depth that is smaller than a depth of the trench.

9. (Previously Presented) The method of claim 8 wherein the step (d) further comprises:

providing O_2 at a flow rate from about 100 to 1000 sccm;

maintaining a chamber pressure at about 5 to 200 mT; and

applying a cathode bias power between 100 and 400 W.

10. (Original) The method of claim 1 wherein the step (d) further comprises:

forming on the cap layer a second patterned etch mask to define the trench; and

stripping the second patterned etch mask contemporaneously with etching the masking material.

11. (Original) The method of claim 1 wherein the step (d) further comprises:

using a very high frequency (VHF) high-density plasma and a selectively controlled cathode bias power.

12. (Original) The method of claim 11 wherein the VHF is about 160 MHz.

13. (Previously Presented) The method of claim 12 wherein the cathode bias power is applied in a range from 0 to about 3000 W at a frequency in a range from about 50 kHz to 13.6 MHz during at least a portion of step (d).

14. (Original) The method of claim 11 wherein the step of etching the cap layer further comprises:

providing CF_4 and N_2 at a flow ratio CF_4:N_2 in a range from 1:1 to 1:5;
applying a source power between about 0 and 2000 W; and
applying a cathode bias power between 400 and 1200 W.

15. (Original) The method of claim 11 wherein the step of etching the trench further comprises:

providing CF_4 and N_2 at a flow ratio CF_4:N_2 in a range from 1:1.2 to 17:1;
applying a source power between about 1000 and 2000 W; and
applying a cathode bias power between 800 and 1800 W.

16. (Original) The method of claim 11 wherein the step of etching the masking material further comprises:

providing O_2 at a flow rate from about 300 to 1000 sccm;
maintaining a chamber pressure at about 5 to 200 mT;
applying a source power between about 200 and 2000 W; and
applying a cathode bias power between 100 and 400 W.

17. (Previously Presented) The method of claim 11 wherein the step of etching the second barrier layer further comprises:

providing CF_4 and N_2 at a flow ratio CF_4: N_2 in a range from 1:5 to 10:1;
applying a source power between about 200 and 600 W; and
applying a cathode bias power between 200 and 400 W.

18-39. (Cancelled)

40. (Previously Presented) A method of etching, comprising:

(a) providing a substrate having a dielectric layer to be etched on a substrate support in a process chamber, the process chamber having a plasma source electrode disposed above the substrate support and a substrate bias electrode disposed below a support surface of the substrate support;

(b) providing an etch gas mixture; and

(c) supplying a source power of at least about 1000 Watts at a frequency of above about 100 MHz to the plasma source electrode and a bias power of at least about 800 Watts to the substrate bias electrode while etching the dielectric layer.

41. (Previously Presented) The method of claim 40, wherein the dielectric layer comprises at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass.

42. (Previously Presented) The method of claim 40, further comprising:

maintaining a chamber pressure greater than about 100 mT.

43. (Previously Presented) The method of claim 40, wherein the chamber pressure is about 250 mT.

44. (Previously Presented) The method of claim 40, wherein step (c) further comprises supplying the source power at about 1,000 watts.

45. (Previously Presented) The method of claim 40, wherein step (c) further comprises providing the bias power at about 1,800 watts.